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ARTICLE

Development of a digital amplifier system for cut-open oocyte electrophysiology

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ABSTRACT The cut-open oocyte Vaseline gap technique is a powerful electrophysiological method for the characterization of ion channels. However, traditional amplifiers for cut-open oocyte Vaseline gap are labor intensive and require significant user expertise. We introduce an innovative, open-source digital amplifier system with high-speed digitization and software-controlled electronics for computer-driven automation. This system compares well to existing commercial systems in terms of conventional specifications of step response (current peak at 25 μs and decay of 36 μs time constant), current noise (1.0 nA at 3-kHz bandwidth), and dynamic range (96.9 dB). Additionally, it unlocks new methods through close integration of the amplifier and software, including machine-learning techniques for tuning capacitive compensation waveforms, achieving a 100-fold suppression of mean-squared transient current, and impedance measurement methods to identify system components such as membrane capacitance and electrode resistances. For future extensions, the design has unique attributes such as real-time digital signal processing for feedback, multiple input and multiple output, and allows for user customization. By providing open-source access to the circuit board designs, control software, and field-programmable gate array code on GitHub, this approach aims to foster cross-disciplinary collaboration and facilitate instrument customization enabling previously inaccessible electrophysiology experiments.

WHY IT MATTERS Ion channels and transporters are critical components of the nervous system, and their electrophysiological characterization plays an essential part in understanding many neurological diseases. Voltage-clamp techniques use an amplifier system to characterize ion channel electrical behavior. Specific voltage-clamp techniques are challenging, partly because the commercial amplifier options are manually operated and require considerable user experience. We present the development of an open-source amplifier system that integrates digitization with software-controlled electronics to simplify the operation and enhance repeatability. Our approaches to capacitive compensation leverage machine learning, providing new methods transferable to other electrophysiology amplifier systems. The amplifier design is open source and provides biophysicists with new options to consider when developing electrophysiological instrumentation for future biological experiments.

INTRODUCTION

Electrophysiology experiments benefit from automated amplifier systems that perform setup, calibration, and acquisition with minimal user interaction. Although automated systems for patch clamp are available (1–4), the market for niche methods such as the cut-open oocyte Vaseline gap (COVG) experiment targeted here is smaller. Consequently, commercial options are limited, and the existing systems require considerable user intervention. Alternatively, an open-source amplifier may encourage cross-disciplinary training, enable creative experiments that require firmware or hardware modifications, and prevent vendor lock-in (5–7). Furthermore, an amplifier system that integrates digitization with software-controlled electronics may accomplish calibrations automatically and leverage digital signal processing for real-time feedback. We have developed a set of amplifier boards and a data acquisition (DAQ) system controlled by a field-programmable gate array (FPGA) for multi-electrode electrophysiology. The

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schematics, software, and firmware of the design are all open sourced so that others may use the tools to develop new electrophysiology instrumentation and apply the system to biological experiments. In this manuscript, we demonstrate amplifier performance when configured for COVG and propose unique calibration and compensation approaches that rely upon the digital architecture of the amplifier and leverage modern machine learning.

COVG is a voltage-clamp technique used to characterize the electrical behavior of ion channels in cell membranes that provides a unique combination of high speed/low noise needed to resolve fast protein dynamics and the rare ability to control both intra- and extra-cellular solutions (8,9). Thus, COVG offers some considerable advantages over the traditional two-electrode voltage-clamp (TEVC) technique. Typically, *Xenopus* oocytes are favored for their low expression of endogenous channels, enabling the introduction of exogenous mRNA for ion channel recordings. However, some fast-gating ion channels produce small current amplitudes that may only be measurable in the low-noise environment offered by COVG. Despite these advantages, experimentalists regard the COVG technique to be challenging because manually operating the amplifiers requires considerable experience and skill. The modern digital electronics amplifier approach presented here facilitates the transfer of much of the configuration and calibration to software, thus producing an easier-to-use amplifier system with advantageous performance characteristics.

COVG presents a notable capacity for studying small-amplitude currents generated by membrane transporters and pumps, which do not produce the large, rapid ionic fluxes typical of ion channels (10). In the COVG configuration, approximately one-sixth of the membrane's surface area is exposed, which reduces the capacitive artifact and minimizes space-clamp artifacts, which are particularly problematic in resolving in fast gated channels such as voltage-gated sodium channels and A-type potassium channels. One of the unique advantages of COVG compared to traditional TEVC is the improved ability to manipulate the ionic composition on either side of the membrane, allowing for better control of conditions that may alter the activity of diverse transport proteins. This control of the ionic environment also enables the measurement of internal fluorescently labeled cysteines (11) and allows electrophysiologists to understand internal conformational rearrangements in the sub-millisecond time domain (12). Despite its potential, COVG has not yet been thoroughly employed to study low-current transporters, ionic pumps, or channels with mutations that reduce conductance. By leveraging the noise reduction and speed enhancements of COVG, it becomes practical to investigate these biological channels with enhanced precision.

For small micrometer-sized "patches" of membrane and compact cells, a single electrode on each side of the membrane simultaneously measures voltage and supplies current as exemplified by the patch-clamp technique. Patch-clamp amplifiers include circuitry to compensate for electrode capacitance and access resistance (13,1) and have been implemented as an integrated circuit for massively multiplexed measurements (2). Specific improvements and compensations for patch clamp include the Giga-Seal approach (14), feed-forward super-charging (15), and series resistance compensation (16) with a state membrane estimator series resistance method for whole-cell patch clamp (17). Amphibian oocytes are a common electrophysiology platform with larger current and capacitance that requires alternatives to patch clamp. The TEVC amplifier is user friendly and supports oocyte measurements (18), yet may be too slow to resolve the fastest dynamics and is limited by spatial inhomogeneity of the membrane voltage (19). These limitations are minimized in COVG, a refinement of the TEVC technique. In this technique, a portion of the oocyte is "cut-open" (generally by saponin permeabilization) to allow for solution exchange, noise reduction, speed increase (20,21), and more uniform control of the membrane voltage. A COVG amplifier was developed and described in (8,22), commercialized by Dagan as the CA-1B (23), and is detailed further in (9,24). The Dagan CA-1B amplifier system uses analog feedback loops and is manually configured through rotary dials and switches. The commercial Sutter dPatch is an FPGA-based digital amplifier system for patch clamp that eases setup with digital sampling and automated compensations of electrode and cell capacitance (3). A similar digital-based amplifier system is not commercially available for the multi-electrode COVG technique.

Measurement artifacts caused by series resistance and transient capacitive currents are challenges encountered by electrophysiologists. Series resistance includes the electrical impedance between the electrode end and the membrane due to the intracellular milieu and creates a time constant $(\tau = R_s C_m)$ that constrains the voltage-clamp speed and may remove important kinetic data (8). In previous work, we demonstrated real-time feedback using digital signal processing to compensate for series resistance (25). In this manuscript, we focus on methods to null capacitive transients so that larger steps of the membrane voltage can be made without saturation of the measurement circuitry.

Sudden changes of the cell membrane voltage cause brief currents known as transient capacitive currents.

To prevent saturation of the electronics due to this transient current, some amplifiers compensate by injecting charge through an auxiliary electrode that bypasses the current-measuring circuit. Capacitive transients may also be removed off-line through the P/N technique by averaging null sweeps (26). However, this technique does not prevent measurement circuit saturation and requires the capacitive current to be linearly dependent on the command voltage. Potential problematic nonlinearities include nonohmic electrode responses and voltage-dependent membrane capacitance due to electrostriction and spontaneous polarization (27). The Dagan CA-1B amplifier (Dagan Corporation, Minneapolis, MN) injects charge through an auxiliary electrode for capacitive compensation. The injected charge is tuned using six rotary knobs that configure three first-order filters, each with an adjustable time constant and an amplitude, and a seventh knob for a global phase adjustment. The process of manually tuning the controls for capacitive artifact mitigation demands both precision and time, and may still not be ideal. Overcompensation can introduce overshoots or oscillations and instability in recordings. Likewise, undercompensation distorts the current-voltage relationship and may bury subtle current changes due to drugs or mutations that affect channel kinetics or voltage dependence. An improved, automated method for adequately compensating for capacitive artifacts would improve the quality of recordings, improve the analysis of ionic or gating current data, minimize the time required for setup, and make experimental results less dependent upon user-selected tuning techniques.

In this work, we present the design and evaluation of a digital-based amplifier platform for research developments in multi-electrode electrophysiology. The amplifier design 1) supports modern state-space control system feedback approaches, 2) enables automated system calibration without user intervention, and 3) is open sourced and thus facilitates custom experiments that require hardware, software, or firmware modifications. This manuscript contributes unique methods enabled by the amplifier design. We develop and validate deconvolutional methods for cancellation of capacitive transients and demonstrate methods for impedance measurement of the electrodes and the cell under test. These impedance measurements of the system under test allow for more accurate configuration of feedback controllers.

System design

Digital amplifier system

We developed a custom DAQ system (Fig. 1 *d*) centered on an FPGA to enable high-speed digitization, rapid data transfer via USB 3.0 to a host computer, and real-time feedback with latency around 1 μs. Design details are presented in (25). The modular design supports up to four HDMI-connected daughter cards, each provided an analog-to-digital converter that samples at 5 megasamples per second (Msps) at 16-bit resolution and two additional voltage measurement channels that sample at up to 1 Msps at 16-bit resolution. The daughter cards also feature configurable peripherals such as relays, analog switches, and slow digital-to-analog converters (DACs), managed through an I2C interface. The FPGA's high-bandwidth DDR memory is used for loading command waveforms, supporting six channels of high-speed DACs that update at 2.5 Msps with a looped duration of 5.87 s. The DDR memory also buffers digitized signals, ensuring continuous data transfer to the host computer without interrupting the experiment or causing temporal gaps.

Amplifier boards and model cell

Three types of custom analog circuit boards, as shown in Fig. 1*c*, were developed and tested. A clamp amplifier (see Fig. 2), creates a high-gain feedback loop that tracks an input voltage, V_{CMD}. The board includes a programmable current-resolving resistor (R_F) to measure the membrane current. The resistor value was made configurable to trade sensitivity and saturation current. The voltage across resistor R_F is amplified by an instrumentation amplifier and then buffered to a 16-bit 5-Msps analog-to-digital converter (ADC) on the DAQ board. This amplifier board supports a sense-force electrode pair (i.e., P1 and P2) as well as a capacitively coupled (CC) terminal to inject charge to the membrane while bypassing the current measurement circuit to mitigate saturation during large transients. The electrode connections are made flexible by relays (see the section "impedance characterization"). A copy of the same clamp board is used to establish a "guard clamp" that keeps the membrane of the middle pool at the same voltage as the top pool by a sense-force pair at GS1 and GS2, as shown in Fig. S1. An independent high-speed DAC sends a command signal to this guard clamp, which, in our model cell testing, tracks the $V_{CMD}(t)$ signal sent to the bath clamp. When testing a biological system, offset voltages between the top pool and the guard pool may be nulled by adding an offset between the digital command signal sent to the bath clamp and command signal for the guard clamp.

A second voltage-clamp board is designed for a low input capacitance to sense the voltage deviation of the bottom plate of the membrane capacitor and create a feedback loop that regulates this voltage to 0 V. This voltage-clamp amplifier includes a programmable offset DAC that allows for nulling voltage offsets

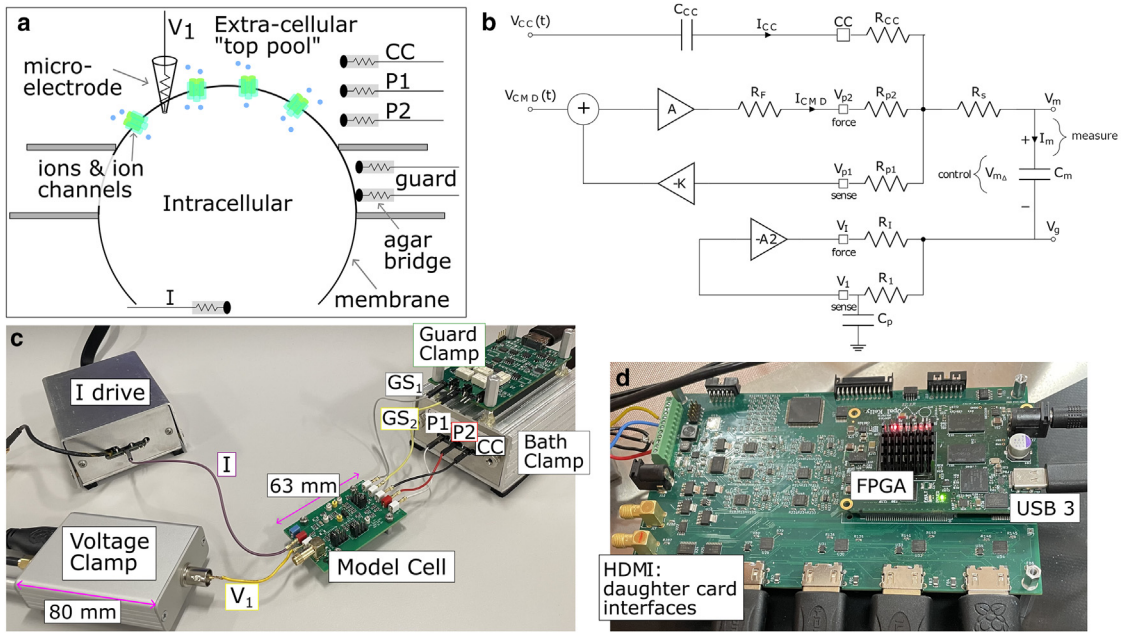

FIGURE 1 System overview. (*a*) The COVG method measures the current through ion channels in the cell membrane of an oocyte. The method permeabilizes the oocyte bottom for access to the intracellular solution (via the I electrode). (*b*) The P1 and P2 electrodes form a sense/force pair that clamps the extra-cellular side of the membrane to a command voltage (V_{CMD}). The V_1 microelectrode pierces the membrane to monitor the intracellular membrane voltage, which is controlled by the *I* electrode. (*c*) Four amplifier circuits (daughter cards) are shown that connect to a model cell for development and evaluation. The model cell emulates the electrode resistances and the electrical properties of the cell membrane. The voltage-clamp board has a BNC input to connect to a microelectrode holder (at V_1) and has a post that extends from the back for mounting to a micromanipulator. Wires are labeled to match the electrode names in *b* and Fig. S1. A dimension of each of the model cell and the voltage-clamp enclosure are included for a sense of scale. (*d*) The amplifier boxes connect to a data acquisition (DAQ) board with analog-to-digital converters (ADCs) that digitize membrane measurement signals (i.e., I_m) and digital-to-analog converters (DACs) to generate control signals (i.e., $V_{CMD}(t)$). The ADCs and DACs are controlled by an FPGA with a USB 3.0 interface to a host computer.

created by the electrodes. A third board is a model cell composed of resistors and capacitors that mimic the electrical properties of the experimental setup including the oocyte capacitance and leak resistance, and various electrode resistances. A complete schematic, including the guard portions, is shown in Fig. S1 and nominal component values for the model cell are included in the supporting material. These boards were designed using KiCAD software and their versions are managed on GitHub. The Supporting material includes links to each GitHub repository with DOIs that link to the board versions used in this manuscript.

FPGA and software

Our work includes significant developments in both the FPGA and host computer software. The FPGA is equipped with various communication controllers to manage peripherals such as analog switches and relays, program DACs, and capture data from ADCs (25). The host computer software is written in Python, utilizing the pyripherals package to streamline and manage communication with these many peripheral devices (28). Experiments are typically conducted using Python scripts executed in an IPython interactive terminal for flexibility (29). For electrophysiology experiments, protocols are loaded into the amplifier system via a comma-separated values spreadsheet, detailing the starting voltage, voltage changes for each sweep, and the duration of each sweep segment. All configuration parameters and experiment details are archived in metadata along with the current and voltage data using HDF5 files (30) for analysis using custom Python scripts. The data can be exported to the Axon Binary Format (ABF), a common format in electrophysiology that is compatible with pClamp (Molecular Devices, San Jose, CA). We have also adapted the pyABF package (31) to enable saving data from our digital amplifier as ABF files. Before saving ABF files, the sampling rates of digitized signals are equalized by decimating the fast ADC current measurements to match the sampling rate of the diagnostic ADC.

MATERIALS AND METHODS

Step response

The dynamic performance of the full amplifier system of Fig. 1 *c* is evaluated while connected to a model cell board by applying step

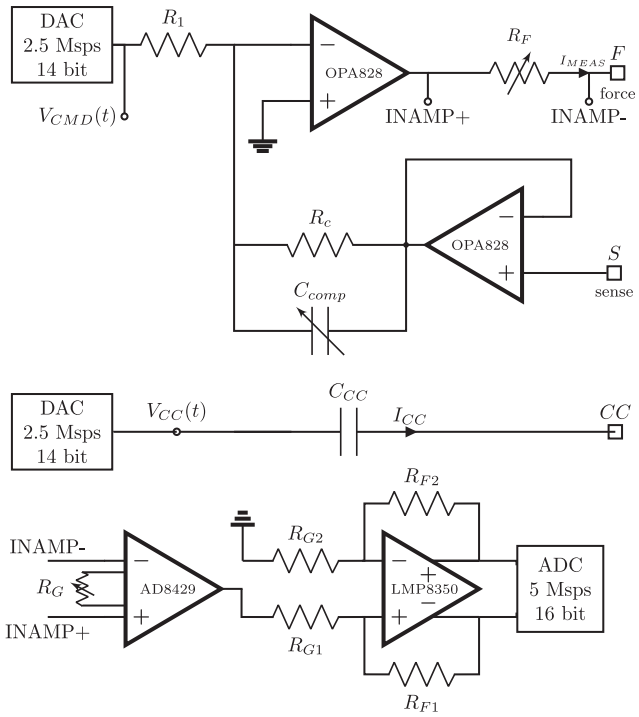

FIGURE 2 Clamp board schematic. The clamp board schematic along with important data converters. F, S, and CC connect to the system under test. All variable resistors and capacitors are controlled by the host computer through I2C writes to I/O expanders that configure digitally controlled switches. The two DACs and the ADC are placed on the DAQ board, which connects to each clamp board by an HDMI cable. Relays for calibration, disconnecting nodes, and shorting F and S are not shown. The same board design is used for both the bath clamp and guard clamp. Each has a separate HDMI connection to the DAQ board and can be separately configured.

functions of various amplitudes to the V_{CMD} terminal. We test the performance for a set of configurations that vary the sensing resistor R_F and the clamp amplifier speed. The speed, fast or slow, is set by adjusting a compensation capacitor (C_{comp}) using programmable analog switches. The DAQ system digitizes I_{MEAS}, the voltage at *P*1, and other diagnostic terminals (*V*1, *I*). In post-processing, I_{MEAS} can be digitally filtered; unless otherwise noted, we use a fifth-order Bessel low-pass filter with a 100-kHz cutoff. Leak current and other sources of current offset are removed during data analysis by subtracting the average current from a time range far from a command step. The total integrated charge versus time is found by trapezoidal integration of the membrane current; with the nominal model cell membrane capacitance value of $C_m = 33$nF, we anticipate around 1 nC per 30 mV of voltage step. Step-response performance metrics are extracted using the Python-control library (32). Rise time (t_r) is evaluated from 10% to 90%, settling time (t_s) is time to within 2% of the steady-state value, and overshoot (OS %) is the percentage of the peak relative to the steady-state value.

Noise and dynamic range

We evaluate the noise of the membrane current measurement using a waveform of 630- ms duration with the current digitized at a sampling rate of 5 Msps and the CMD signal held steady. For noise investigations, important configurations include the sensing resistor, R_F, the instrumentation amplifier gain, and the clamp amplifier speed. The total root mean square (RMS) current noise for a given measurement bandwidth, $I_n(f_{BW})$, is the standard deviation of the membrane current after processing by a fifth-order low-pass Bessel filter with a cutoff frequency of f_{BW}. The noise power spectral density, $P(f)$, is calculated using Welch's method (from scipy.signal) with 8192 sample points per segment. The integrated noise as a function of the high-frequency bandwidth (f_H) is

$$I_{nI} = \sqrt{\int_{f=f_L}^{f=f_H} P(f)df} \tag{1}$$

where f_L is the lowest measured frequency set by the waveform length. Current noise is compared to the peak current without saturation I_{pk} for a given configuration to establish a dynamic range as $DR = I_{pk}/I_n$ (see Fig. S3 for measures of peak current versus voltage step).

Capacitive compensation via impulse response deconvolution

Capacitive compensation uses an auxiliary electrode to source charge so that the current measuring circuit does not saturate during a large step change of the membrane voltage. Referring to Fig. 1 *b*, the membrane current is

$$\begin{aligned} I_m(t) &= I_{MEAS}(t) + I_{CC}(t) \\ &= h_{CMD}(t) * V_{CMD}(t) + h_{CC}(t) * V_{CC}(t) \end{aligned} \tag{2}$$

where $h_x(t)$ is the impulse response of terminal *x*, $V_x(t)$ is the applied waveform at terminal *x*, and $*$ is the convolution operator. A conventional amplifier system utilizes a set of analog filters with manually tuned gain and phase that filter the V_{CMD} signal to generate a V_{CC} waveform that minimizes the current that flows through the current measurement circuit (R_F) during the capacitive transient. In this work, we apply the flexible signal processing and automated tuning capabilities of the digital amplifier system to capacitive compensation. To do so, we measure the impulse response of each terminal and then generate *CC* voltage waveforms by deconvolutional methods that null $I_{MEAS}(t)$. Two methods are developed and assessed: 1) noncausal signal processing that calculates the $V_{CC}(t)$ waveform before the beginning of an experiment, and 2) a causal filter *H* for FPGA implementation and real-time processing with $V_{CC}(t) = HV_{CMD}(t)$. Both methods require a measurement of the impulse response at each terminal. We measure these impulses by applying a step input and calculating the derivative of the measured current. For the measurement of the CC impulse response, V_{CMD} is held constant so that the membrane voltage does not change and $I_{CC}(t) = -I_{MEAS}(t)$, which can be measured by the current measurement circuit that monitors R_F. For simplicity, experimental measurements of the proposed capacitive compensation methods do not include the guard clamp amplifier.

The first method learns a $V_{CC}(t)$ by cubic spline interpolation using a Python package that provides differentiable cubic splines (33) compatible with the PyTorch machine-learning library. We use a cubic B-spline with 50 control points. The B-spline enforces continuous second derivatives to ensure that the resulting waveform is feasible to produce with the DAQ circuitry. The spline parameters are optimized to minimize a loss function of the mean square error between the measured membrane current induced by a command waveform step and the current produced by the compensation terminal predicted as $h_{CC} * V_{CMD}(t)$. Optimization is done using ADAM (34) with a learning rate of 10^{-3}.

A second method develops a causal filter that operates on $V_{CMD}(t)$ to calculate $V_{CC}(t)$ in real time. This method enables the compensation waveform to respond to dynamic command waveform

adjustments, such as series resistance compensation to minimize the shaping from the combination of the series resistance (R_S) and membrane capacitance (C_m). The filter architecture follows the general structure used by conventional COVG amplifiers. Our total filter is the composite of low-pass (H_L), high-pass (H_H), and all-pass (H_A, for delay) filters each with separately learnable parameters of cutoff (or center) frequency, Q, and gain. The total filter passes the sum of the low-pass and high-pass outputs through the all-pass delay as $H = H_A(H_{L1} + H_{L2} + H_H)$. More complex architectures are possible at the cost of FPGA implementation complexity and training time. The FPGA signal processor of our digital amplifier system supports infinite impulse response filters constructed as biquads. So that the parameters of each filter can be learned, we use differentiable biquad elements implemented for the PyTorch machine-learning library (35) in the Torchaudio library (36). The learned filter, H, is trained using ADAM (34) with a learning rate of 10^{-3} to minimize a loss function of the mean square error between the measured membrane current induced by a command waveform step and the estimated current produced by the compensation terminal, $h_{CC} * (HV_{CMD}(t))$.

Impedance characterization

For electrode calibration and impedance characterization of the cell under test, the force-sense electrode pair ($P2$ and $P1$) on the clamp board is equipped with five relays. Each electrode is connected to two relays: one for linking or detaching the electrode from the amplifier loop and another for connecting or disconnecting it to an isolated diagnostic terminal. The diagnostic connections can inject or measure signals with several configuration options: grounded, floating, connected to the input of an analog-to-digital converter (ADS8686), a voltage source, or a current source—both sources have arbitrary waveform generation. A fifth relay is shared between both electrodes and, when closed, connects $P2$ and $P1$, thus bypassing the feedback loop that is established by the electrodes and chamber solution in standard operation. The injected voltage and current waveforms are generated by an eight-channel 16-bit DAC with 5 $-$ μs settling time (DAC80508), which is updated by the FPGA via SPI at a rate up to 2.5 MSPS. The current source is an advanced Howland topology (37) with a resistor configurable full-scale range with a default configuration that produces a full-scale current amplitude of 1.6 μA.

P1/P2 electrode resistances are extracted in two steps. First, a direct current (DC) input is applied as shown in Fig. S6 to determine the sum of the two resistances. The digitized voltage across the resistors is fit to a "soft" square wave of the form $A \tanh(s \cos(2\pi ft + \phi))$ so that the RC shaping of rise and fall does not cause error in the estimated amplitude. For the square wave, A is the amplitude, s controls the shaping, f is the known wave frequency, and ϕ is the phase. Second, to determine individual resistances, we measure two transfer functions using an injected chirp signal as shown in Fig. S7. At each frequency, the measured frequency is found by quadratic interpolation of the maximum spectral peak, the amplitude is calculated from the waveform standard deviation, and the phase is determined by cross-correlation of the input and output sinusoids. The measured transfer functions are fitted to an analytical transfer function model using a nonlinear least-squares minimization library, LMFIT (38), to extract component values, including R_{CC}. The transfer function model for the P2/P1 electrodes with the CC drive held at a small signal ground is

$$H_b(\omega) = \frac{j\omega R_{CC} C_{CC} + 1}{j\omega (R_{CC} + R_{Px}) C_{CC} + 1} \tag{3}$$

where R_{Px} is the resistance of the electrode onto which the signal is injected, C_{CC} is a known value (4.7 nF), and $\omega = 2\pi f$. The V_1 and V_I electrodes are floated for this measurement to eliminate the uncertain electrical properties of the cell membrane and chamber solutions.

Similarly, a chirp signal is applied to the I terminal with both $P1$ and $P2$ electrodes grounded. With R_{p1} and R_{p2} determined in earlier measurements, the measured transfer function can be fitted to

$$\begin{aligned} \xi &= \left(\frac{1}{sC_{CC}} + R_{CC}\right) \| (R_{P1} \| R_{P2}) + R_s + \frac{1}{sC_m} \\ H_c(s = j\omega) &= \frac{\xi}{\xi + R_I} \end{aligned} \tag{4}$$

to estimate R_I and the membrane capacitance C_m.

The V1 sense terminal is a special case as the resistance of this microelectrode is large, on the order of 500 kΩ, such that the parasitic capacitance C_p at this node must be minimized for wide bandwidth feedback. To minimize the parasitic capacitance, we omitted a relay for diagnostic connections, which means that DC can be neither sourced nor sunk at node V1. Instead, we measure the step response of this node. To do so, the feedback loop formed by amplifier $A2$ is broken at I and a voltage step is applied to the I electrode. The output of amplifier A2 is digitized and the RC time constant extracted for an estimate of $R_1 + R_I$. For this method, the amplifier input capacitance is separately measured. The microelectrode will contribute an additional and unknown parasitic capacitance, yet this method still provides an estimate of the microelectrode resistance and health. When a COVG chamber is used for biological experiments, this electrode characterization step requires the V1 microelectrode to be placed in solution with the I electrode. In a separate measurement, a top-pool bath electrode (P2 or P1) is used to determine R_I following the DC pulse procedure of S6. For simplicity, experimental measurements of the proposed impedance characterization methods do not include the guard clamp amplifier.

RESULTS

Step response

The sensing resistor value determines the maximum voltage step that can be measured without saturation. For values of $R_F = 33, 100, 332,$ and 1000 kΩ the saturation voltage is approximately 320, 120, 100, and 20 mV for the fast response configuration. A comprehensive figure and more analysis is included in Figs. 3 and 4 of the supporting material. Table 1 shows that the rise time of the voltage at P1 and the peak time of the current is faster than the limiting time constant of the access resistance ($R_s C_m$). The time constant, τ, of the membrane current decay of the fast configurations is about 36 μs, which demonstrates that the dynamics are dominated by the model cell ($R_s C_m = 33.3$ μs) and are not considerably slowed by the amplifier. The measured current decay rate for the fast configurations is similar to values reported for other COVG amplifiers as 20–100 μs (23) and 20–40 μs (22).

At higher sensitivities, the fast response is underdamped; the slow response stabilizes the higher sensitivity configurations at the cost of slower rise time. Note that the voltage at P1 tracks but is not precisely the voltage at the membrane because of the

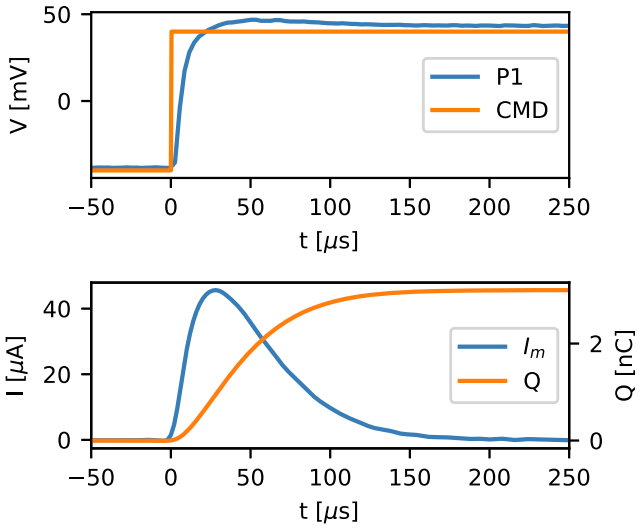

FIGURE 3 Step response (fast response configuration). Top: commanded voltage step of 80 mV (CMD) and the digitized response at the P1 electrode with $R_F = 100$ kΩ and a fast response speed. Bottom: capacitive current and integrated charge in response to the command step processed off-line with a 100-kHz cutoff digital filter.

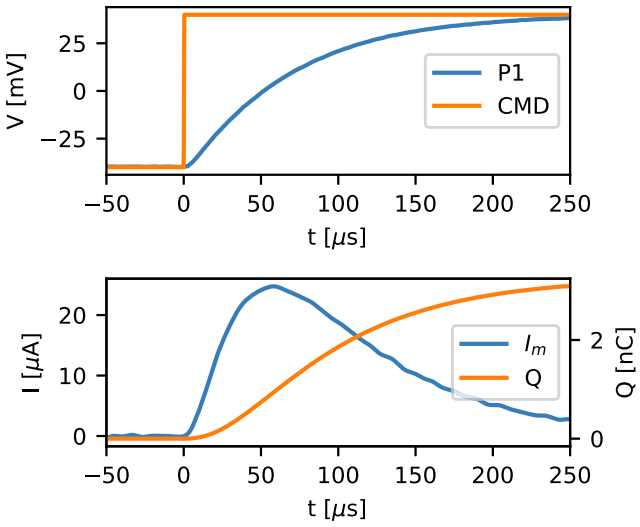

FIGURE 4 Step response (slow response configuration). Top: commanded voltage step of 80 mV and the measured response at the P1 electrode with $R_F = 100$ kΩ and a slow response speed. Bottom: capacitive current and integrated charge processed off-line with a 100-kHz cutoff digital filter.

voltage drop across the access resistance from the membrane current ($V_m = V_{P1} - I_m R_s$). Figs. 3 and 4 demonstrate the voltage steps (top) as well as the measured current and integrated charge (bottom) from which the summary measurements of Table 1 are extracted. As an example, the fast configuration shown in Fig. 3 measures a current peak time of 27.6 μs, membrane current $\tau = 36.0$ μs, and settling of the integrated charge in ~ 125 μs.

Noise and dynamic range

Table 2 shows the noise in the current measurement for various configurations and two cutoff frequencies of a fifth-order Bessel filter. When configured with $R_F = 100$ or 332 kΩ sensitivity, this amplifier achieves noise performance of 1.0 nA RMS, which is similar to previous work (1 nA RMS at 3 kHz (23) and 1.2 nA RMS at 5 kHz (22)). Fig. 5 displays the integrated noise to elucidate the relationship between noise and measurement bandwidth. Total noise increases up to a bandwidth of around 100 kHz and then plateaus due to the roll-off of the amplifier loop. The integrated noise method effectively applies a brick wall filter without any in-band attenuation so the Bessel filter and standard deviation approach of Table 2 reports lower values. The 100 kΩ configuration is suited for general-purpose measurements with a peak current of 70μA (see Fig. S3) and an RMS noise of 1.0 nA for a dynamic range of 96.9 dB and allows for a membrane voltage swing of 100 mV before saturation (without capacitive compensation). The noise limit as set by passive components (i.e., membrane capacitance and electrode resistances) with ideal clamping op-amps was simulated in SPICE and is indicated as a dashed line in Figs. 5 and S5. The simulated current noise integrated up to 3 kHz is 1.03 nA RMS with a primary contribution from the thermal noise of R_1 (the resistance of the micropipete). An analytical expression for this noise is included in the supporting material. The integrated noise of the total amplifier system is $\sim \times 2$ the noise floor as set by the model cell, which shows that the

TABLE 1 Step-response analysis for multiple amplifier configurations

Configuration		V_{P1}			I_m	
R_F [k Ω]	Speed	t_r [μ s]	OS %	t_s [μ s]	t_{pk} [μ s]	τ [μ s]
33	fast	9.0	3.1	80.6	25.6	37.5
100	fast	12.0	7.7	119.6	27.6	36.0
332	fast	60.0	14.2	185.6	45.6	36.2
1000	fast	30.0	28.2	365.6	65.6	59.8
100	slow	138.0	0.3	287.6	73.6	103.7
332	slow	120.0	0.1	275.6	85.6	134.9
1000	slow	120.0	2.6	365.6	105.6	188.4

Steps of 80 mV and 10 mV are used for $R_F < 332$ kΩ and $R_F \geq 332$ kΩ, respectively. Before step-response analysis, waveforms are filtered with a fifth-order Bessel filter with center frequency of 100 kHz ($R_F < 332$ kΩ) or 10 kHz ($R_F \geq 332$ kΩ). All measurements are with an instrumentation amplifier gain of $\times$ 2. For the measured current (I_m), t_{pk} is the time of peak current. τ is the time constant of membrane current exponential decay as evaluated by a nonlinear fit to I_m from $t_{pk} + 30$ μs to $t_{pk} + 200$ μs. Unstable R_F and speed combinations are removed.

TABLE 2 Noise of the measured current determined by the standard deviation of a 630-ms measurement calculated after filtering with a fifth-order Bessel filter of cutoff frequency (f_c)

Configuration		RMS I_m noise [nA]	
R_F [k Ω]	Speed	f_c = 10kHz	f_c = 3kHz
33	fast	5.4	3.0
100	fast	4.7	1.0
332	fast	4.6	1.0
332	slow	4.0	1.6
1000	slow	3.6	2.2

op-amps, current-resolving resistor, and digitization contribute modestly but do not dominate the total noise.

Capacitive compensation

Fig. 6 shows measured impulse responses (see Eq. 2), which are determined from the measured current in response to a step applied to the CMD and CC terminals.

The model cell component values are intentionally adjusted away from nominal (R_S = 500 Ω) to induce undershoot in the I_m response, which is a more challenging transient to compensate. Fig. 6 displays these impulse responses after a 500-kHz first-order low-pass filter. Fig. 7 (top) shows the measured current from a CMD terminal step (I_{CC}) with the simulated I_{CC} from the learned cubic spline interpolation. The inset demonstrates the evolution of the waveform as training proceeds. The optimized compensation waveform is applied experimentally in Fig. 7 (bottom) to produce I_{CC}. When the command step and the optimized compensation waveform are applied together, the total measured current (green trace) demonstrates effective cancellation of the capacitive transient.

Table 3 quantifies the performance of the cancellation measurements evaluated from 50 μs before to 250 μs after the step after filtering the current with a first-order Butterworth filter of f_c = 1MHz. The summary statistics included the squared deviation from zero of the waveform, calculated as $\sum I_m^2$, the absolute peak current (I_{peak}), and the total charge (Q_t). For the first two configurations in Table 3 with fast rise times, the peak current is reduced to 6% or less of the uncompensated waveform. The squared deviation quantifies the quality of compensation at all points and is reduced by $\sim \times 100$ or more for all configurations.

In simulations, we also demonstrated the feasibility of optimizing biquad filters for real-time generation of $V_{CC}(t)$ via filtering of the CMD waveform. Fig. 8 demonstrates the evolution of the resulting compensation waveform during training. The filter training successfully drives down the loss function (inset) and plateaus after around 20 epochs but the CC current does not track the undershoot generated by intentional detuning that occurs around 120 μs after the initial rising edge. The filter would require more degrees of freedom and likely a second and separate delay to capture the undershoot. Future work is required to implement the filters onto the FPGA for experimental measurements.

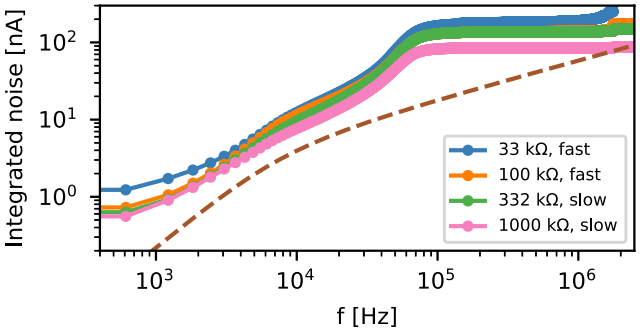

FIGURE 5 Integrated current noise versus frequency. The integrated membrane current noise versus the high-frequency cutoff (see Eq. 1) for four different clamp amplifier configurations. The dashed line shows the integrated noise from the passive components of the model cell combined with ideal clamping op-amps as extracted from a SPICE simulation.

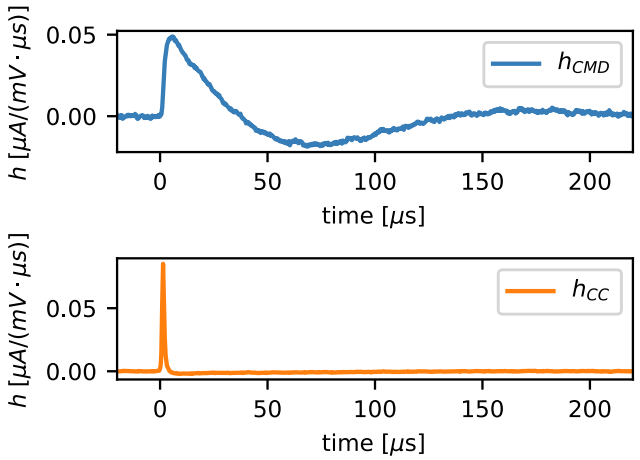

FIGURE 6 Impulse responses. The impulse responses of the sensed current in response to the CMD terminal (top), $h_{CMD}(t)$, and the CC terminal (bottom), $h_{CC}(t)$. Impulse responses are calculated by differentiating the response to a step function.

Impedance characterization

We captured experimental data using the digital amplifier electronics and a model cell to evaluate impedance characterization methods that determine the electrical parameters of components that vary with the cell under test or the recording chamber. The model cell ground-truth values were measured with an LCR meter (LCR-6300, GwInstek). Model cell components R_s, R_{p1}, and R_1 are jumper programmable

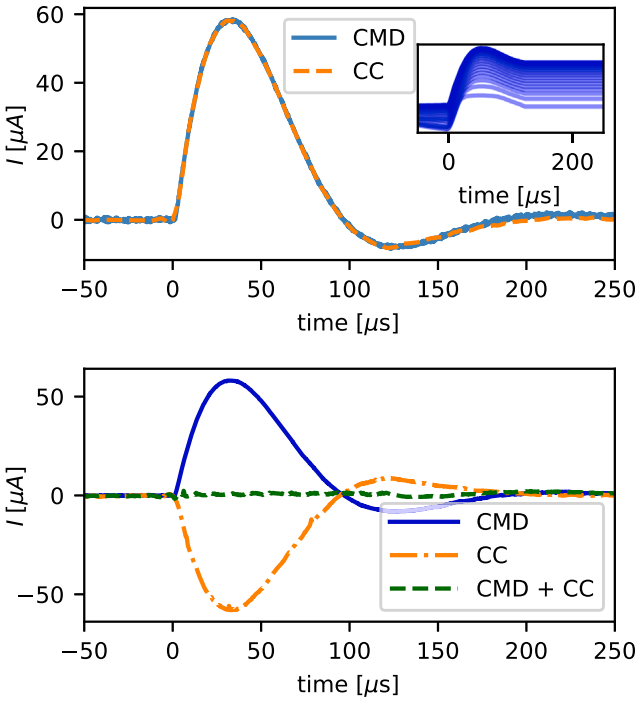

FIGURE 7 Capacitive compensation training. Top: (simulations and training) the current produced by a CC waveform (*dashed orange*) as determined by training of a cubic spline interpolation. The CC waveform is convolved with h_{CC} and the result nulls the current from a step input on the CMD terminal (blue). The CC current is inverted for easier comparison. The inset shows the CC waveform evolution during training with lines darkening as training progresses. Bottom (measurements): the pre-calculated CC waveform is programmed into the FPGA and the cancellation performance is evaluated. The green trace shows the residual current when $V_{CMD}(t)$ and $V_{CC}(t)$ are applied simultaneously with a membrane voltage step of 62.5 mV. The simulations and measurements use a configuration of $R_F = 33$ kΩ and the fast response speed.

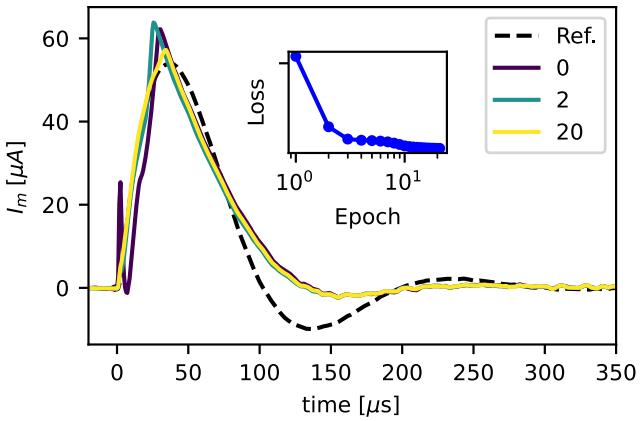

FIGURE 8 Learned filter capacitive compensation. Training results of a learned filter amenable to FPGA implementation (biquads) for capacitive compensation. The compensation currents at a subset of training epochs as indicated in the legend are overlaid upon the reference current as measured from a CMD step response. The inset shows the mean square error (MSE) loss function versus training epoch on a log-log scale. Before training, the MSE is 2.49×10^{-2} and reaches a minimum of 2.5×10^{-3}. The minimum is reached after ~20 epochs.

with four distinct values. The measurement sequence was designed to be compatible with the steps required for an electrophysiology measurement.

The three electrode resistances associated with the top pool are first estimated using a current source step function and then refined using an AC chirp signal. Fig. 9 demonstrates the measured voltage across $R_{p1} + R_{p2}$ with a sourced current of 1.6 μA peak-to-peak square wave. The four ground-truth values of $R_{p1} + R_{p2}$ ranged from 8.298 to 14.995 kΩ and were measured with a maximum relative error magnitude of $-$ 1.36%.

The amplifier boards do not allow for isolating the two resistance values using DC measurements. To separately estimate the values of R_{p1} and R_{p2} and determine the resistance of the capacitive compensation electrode (R_{cc}), we inject a chirp signal and measure the transfer function versus frequency as shown in Fig. 10. The jumper-programmable resistor, R_{p1}, is estimated with an error magnitude of less than 0.95% for each of the four values tested. For the data demonstrated in Fig. 10, the R_{p2} error is $-$ 0.34% and the R_{cc} error is $-$ 2.79%.

The V1 microelectrode voltage-sensing amplifier does not have digitally configurable relays for signal

TABLE 3 Configuration and summary statistics of measured membrane current with and without capacitive compensation at four different configurations with each trained separately

R_F [k Ω]	speed	Undershoot	CC comp.?	Sq. deviation [A^2]	I_{peak} [μA]	Q_t [nC]
33	fast	14.1	no	7.25×10^{-7}	58.7	2.86
33	fast	-	yes	1.77×10^{-9}	3.61	0.186
100	fast	18	no	7.14×10^{-7}	55	2.79
100	fast	-	yes	8.02×10^{-10}	2.01	0.107
100	slow	1.24	no	2.46×10^{-7}	26.7	2.72
100	slow	-	yes	2.21×10^{-9}	3.71	0.259
332	slow	4.51	no	1.51×10^{-8}	6.35	0.687
332	slow	-	yes	1.6×10^{-10}	0.823	0.002 91

The speed configuration trades rise time and undershoot. A membrane voltage step of 62.5 mV was used for all entries except for $R_F = 332$ kΩ, which uses 15.6 mV. CC comp., capacitive compensation.

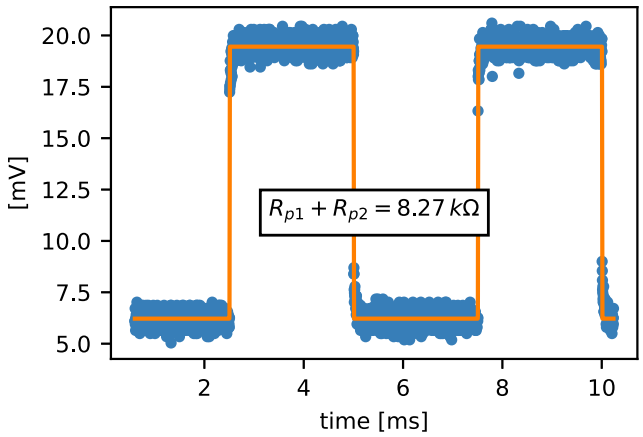

FIGURE 9 Electrode resistance characterization. Pulsed current measurement to determine the total bath electrode resistances, $R_{P1} + R_{P2}$. Data are blue markers with a fit to a soft square wave of the form $A\tanh(s\cos(2\pi ft + \phi))$ shown in orange. Diagnostic relays on the clamp board are configured to disconnect the feedback amplifier and connect a pulsed current source to P1. The same node is digitized by an auxiliary ADC channel with electrode P2 grounded (see Fig. S6). The resistance value extracted from the measurement is 8.27 kΩ as compared to a ground truth of 8.298 kΩ. Since the connection between R_{P1} and R_{P2} is formed within the pool, the two resistances cannot be isolated.

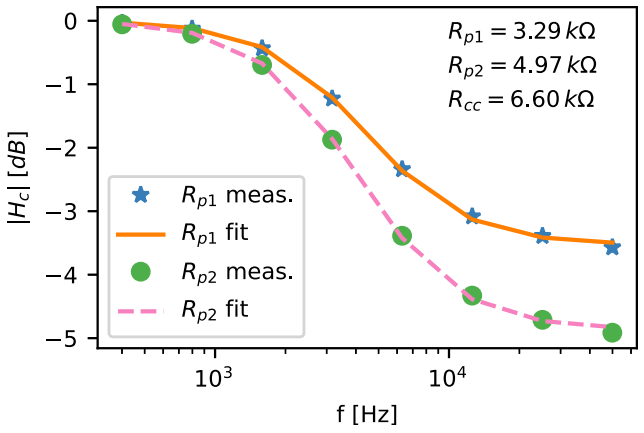

FIGURE 10 Measured system transfer functions. Two measured transfer functions that are measured using a chirp stimulus (see Fig. S7) (*star and circle markers*) with corresponding fits (*solid lines*). The measurements and fits are labeled by the electrode resistance that is driven (i.e., fits the role of R_1 in Fig. S7). Fits to these transfer functions using Eq. 3 extract the three electrode resistances that connect to the top bath (annotated in the top right).

injection or probing, so DC injection cannot be used to measure the electrode resistance. Alternatively, Fig. 11 demonstrates an approach that determines the *RC* time constant of this sensing node. For this measurement, the P1 and P2 electrodes are disconnected by the programmable relays and the CC electrode is disconnected so that the membrane does not add a capacitive load. For R_1 values of 100, 200, 475, and 1000 kΩ, we measure time constants from 4.1 to 10 μs and estimate the parasitic capacitance using the measurements with the largest value to be 9.5 pF. The RC time constant of the smaller R_1 values is increased due to shaping from the amplifier and digitization circuitry. This method allows for estimation of the health of the microelectrode and, with a known amplifier input capacitance (i.e., C_p in Fig. 1 *b*), R_1 may be estimated, yet any additional and unaccounted for distributed capacitance of the microelectrode will cause an overestimation of R_1.

An AC transfer function measurement using a 50-mV amplitude chirp waveform injected through the *I* electrode and sensed at the V_1 node is used to estimate the *I* electrode resistance and the capacitance of the membrane. Fig. 12 shows the resulting measurement and fit to the transfer function of Eq. 4 with the CC elements removed and the series resistance value fixed to $R_s = 1$ kΩ. The membrane capacitance estimate of 35.8 nF is 8.9% greater than the LCR measurement of 32.6 nF, whereas the R_I estimate is below the ground-truth measurement of 94.2 kΩ. These measurements are designed to verify that the experimental setup is properly established and to provide parameters to real-time digital feedback controllers, so high accuracy is not prioritized. Other methodologies, such as paired ramps, may be preferred to minimize the impact of nonlinear membrane I-V due to voltage-dependent activation or inactivation of conductance (39).

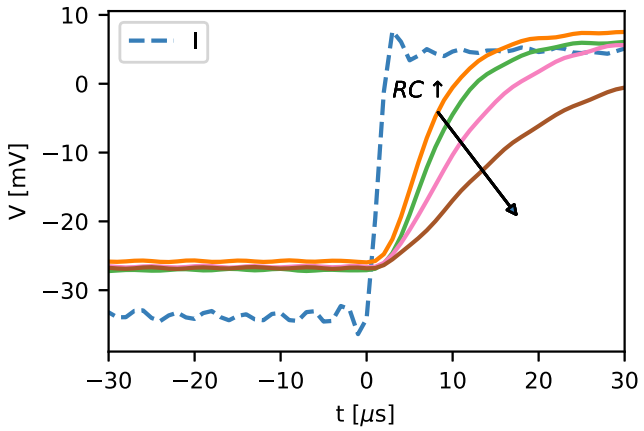

FIGURE 11 Sense amplifier capacitance characterization. A voltage step of 40 mV (*blue, dashed line*) is applied to the *I* electrode for four values of R_1: 100 kΩ (*orange*), 200, 475, and 1000 kΩ (*brown*). The voltage sense amplifier step response verifies the *RC* time constant of the V_1 sensing node to extract the microelectrode resistance. The digitized V_1 signal is scaled by the gain of the amplifier so that the display value is input referred; modest offset voltages are shown and were not nulled since these do not impact extraction of the *RC* time constant.

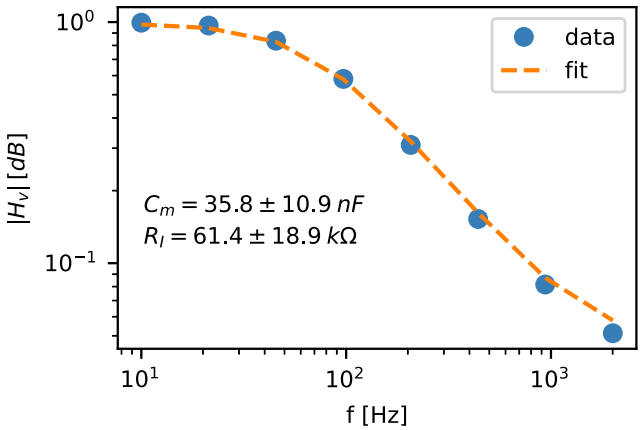

FIGURE 12 Measured transfer function to extract membrane capacitance. Measured transfer function (*circles*) with a chirp applied to electrode I and a corresponding fit to Eq. 4 and uncertainties extracted from the fit error. This transfer function allows for extraction of the driving electrode (I) resistance and an estimate of the membrane capacitance (C_m).

DISCUSSION

This manuscript presents a flexible electronics system for COVG electrophysiology measurements and is open sourced to also allow for user-driven modifications for custom measurements, such as impedance spectroscopy (40,41) or dynamic clamp (42,43). By shifting amplifier configuration to software, and away from manually controlled switches and knobs, this system allows for automated, repeatable, and data-driven setup. We used a model cell to demonstrate a reproducible suite of performance tests and measured competitive specifications for step response (36 $-$ μs current time constant), linearity, and noise (1.0-nA RMS at 3-kHz bandwidth). Furthermore, in this manuscript, we present creative methods for capacitive compensation by learning a compensating waveform constructed from differentiable splines to minimize the residual current calculated from the measured impulse response of the CMD and CC terminals. The diagnostic relays on the amplifier boards and auxiliary ADCs and DACs allow for frequency-dependent impedance characterization that extracts the electrical parameters of the biological setup that may vary from experiment to experiment. These compensation and impedance characterization methods are valuable building blocks for automated setup and tuning of an advanced control system, respectively, that are in development.

Biological measurements represent a critical next step for future work. In the present study, we used a model cell, which offers the advantage of providing reproducible measurements across laboratories due to the known and consistent electrical parameters. However, a model cell does not account for the complexities that arise in biological systems, such as solution-electrode voltage offsets, variability in resistance and capacitance values, fluctuating leakage currents, and nonlinearites of electrode resistances and membrane capacitances. The hardware was designed to address these challenges, but its ability to fully handle them has not yet been validated. To prepare for biological experiments, we need to further organize the software to streamline the setup and ensure tight integration with the experimental procedures (24).

The real-time feedback enabled by the custom DAQ board and FPGA signal processing is well suited for the use of advanced control systems that may offer improved performance over conventional methods such as series resistance compensation (13). The conventional approach for series resistance compensation measures the membrane current and adjusts the commanded voltage by adding the estimated voltage drop across this resistor $(I_m R_s)$. This approach requires an accurate estimate of R_s and can be unstable at high bandwidths. Sherman et al. improved stability for whole-cell patch-clamp measurements by using a membrane state estimator (17). . In the same vein, for future work, we are leveraging the many ADCs and DACs of this system and the low latency digital feedback provided by the FPGA to develop modern control systems design (state space and multi-input multi-output) for COVG, which implicitly includes series resistance compensation. The impedance estimation methods developed in this work are an important building block of system identification to guide feedback controller configuration with known model parameters for improved performance and/or robustness (44).

The automated capacitive compensation developments demonstrate successful training of biquad filters (Fig. 8) that, in real time, can process the command signal to create a compensatory signal that nulls the capacitive transient current. Biquad filters are a natural building block for digital signal processing. However, this method has not yet been implemented on the FPGA or experimentally evaluated. An important next step is to map the software implementation of the capacitive compensation biquads to a hardware implementation on the FPGA. After verifying the FPGA implementation via simulation, we will then test the compensation method using our hardware.

Voltage-clamp fluorometry, which simultaneously records electrophysiology signals and fluorescence data (24), requires measurement synchronization and additional digitization channels. The proposed amplifier has been designed to accommodate such extensions, offering digital inputs and outputs for

synchronization and free analog inputs (ADCs) and analog outputs (DACs) for recording and stimulus control. Due to this flexibility, the system is expected to be well suited for future applications in multi-modal experiments such as voltage-clamp fluorometry. Furthermore, experiments that require unconventional modifications to the electronics, software, and/or firmware may be a particularly good fit.

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AUTHOR CONTRIBUTIONS

Software and firmware, A.S., I.D.B., and L.J.K.; PCB design and testing, L.J.K., J.H., and I.D.B.; methodology, L.J.K. and L.M.B.; design and performance of experiments, L.J.K. and I.S.K.S.; data analysis, L.J.K., I.S.K.S., and L.M.B.; writing and editing, L.J.K., I.S.K.S., and L.M.B.; supervision of undergraduate researchers, L.J.K. and L.M.B.; funding acquisition, L.J.K. and L.M.B.

DECLARATION OF INTERESTS

The authors declare no competing interests.

DECLARATION OF GENERATIVE AI AND AI-ASSISTED TECHNOLOGIES IN THE WRITING PROCESS

During the preparation of this work, an author (L.J.K.) used ChatGPT4 to rewrite certain sentences for clarity and to generate a skeleton of the tikz schematics in the supporting material (Figs. S6 and S7). After using this tool, the authors reviewed and edited the content as needed and take full responsibility for the content of the publication.

SUPPORTING MATERIAL

Supporting material can be found online at https://doi.org/10.1016/j.bpr.2024.100185.

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